

Internship subject (Master 2)

Hardware Compilation: Recover the FIFOs!

Advisor: Christophe Alias, christophe.alias@ens-lyon.fr

Place: Laboratoire de l'Informatique du Parallélisme (LIP)
École Normale Supérieure de Lyon

Context

A process network is a collection of pure functions communicating through channels. Process networks are a natural intermediate representation for hardware compilation: the front-end extracts the parallelism and derive the process network. Then, the back-end maps the process network to hardware. In this internship, we propose to focus on the compilation of *channels* to hardware.

Compiler optimizations for parallelism and data locality restructure deeply the execution order of the program, hence the read/write patterns in communication channels. This breaks most of the FIFO channels, which have to be reimplemented with addressable buffers. Expensive hardware is then required to enforce synchronizations, which often results in dramatic performance loss. We have proposed an algorithm to reorganize the channels [1] so the FIFO broken by a loop tiling can be recovered. We have proven this algorithm to be complete over DPN [2], a constrained family of process networks.

Objectives

The goal of this internship is to study the completeness of FIFO recovery on *general* process networks. Does there exists an algorithm to recover the FIFO broken by *any* tiling transformation? In the positive case (our belief), find an algorithm and prove the completeness. Otherwise, point out the fundamental reasons why such an algorithm can never exists.

- Study several polyhedral programs where the technique developed in [1] did not work, and analyze the causes.
- Propose a complete algorithm + proof of completeness. Or, prove that such an algorithm can never exist.
- In the positive case, implement and test your algorithm. The approach will be validated experimentally on the benchmarks of the polyhedral community [3].

Requirements. Notions in compilers and parallelism

References

- [1] Christophe Alias. Improving communication patterns in polyhedral process networks. In *Sixth International Workshop on High Performance Energy Efficient Embedded Systems (HIP3ES 2018)*.
- [2] Christophe Alias. Fifo recovery by depth-partitioning is complete on data-aware process networks. Technical Report RR 9187, INRIA, June 2018.
- [3] Louis-Noël Pouchet. Polybench: The polyhedral benchmark suite. *URL: [http://www. cs. ucla. edu/~ pouchet/software/polybench/](http://www.cs.ucla.edu/~pouchet/software/polybench/)[cited July,], 2012.*