Intership of Master 2 Recherche
Compiling process networks on GPU

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Duration: 4 – 6 mois. Possible pursuing with a PhD thesis.

Place: Laboratoire de l'informatique du parallélisme, École normale supérieure de Lyon.
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Process networks are an execution model which express naturally the parallelism of a computation. Process networks are a natural intermediate representation for a parallelizing compiler, where the front-end extracts the parallelism of the source program, and the back-end maps the process network to the target architecture.

We have designed a process network model which makes explicit the communications with the central memory, by adapting the algorithm described in the PhD thesis of Alexandru Plesco [1], with the initial goal of compiling efficient circuits on FPGA.

In this intership, we propose to study how to map our process networks to GPU-based harware accelerators. The trainee will:

- study the state of the art on process networks and automatic parallelization, notably on GPU ;
- translate "by hand" several simple process networks (vector sum, matrix multiply, 1D Jacobi, etc) ;
- propose a translation algorithm, and possible improvements to the process model ;
- implement (in C++), test and validate the approach experimentally.

Prerequisite. Strong basis in compilers and computer architecture.

References

[1] Alexandru Plesco. *Program Transformations and Memory Architecture Optimizations for High-Level Synthesis of Hardware Accelerators.* PhD thesis, Ecole Normale Supérieure de Lyon, sep 2010.